A Multifunctional Laser Linking and Cutting Structure for Standard 0.25 µm CMOS-Technology

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Abstract

A novel laser-switch has been developed, designed and manufactured in a standard 6 level metal CMOS process. The redimensioned laser-switches combine a laser link and via (fuse) corresponding to minimum design rules in a single device. Due to vertical arrangement of the linking and the cutting structure (via), an area reduction of more than 30% is achieved, compared to laser arrays utilizing traditional laser structures. Simultaneous connecting and disconnecting reduces the processing time by 50%, since an additional process step is omitted. The resistance of the formed link structures is very low ($R_{12x12median}$=0.065 Ω ,$R_{10x10median}$ =0.118 Ω). Optimal values have been found for laser parameters to process the cutting structure with 100% yield. A first estimation of life-time results in $t_{0.1}$=22 a. Arrangements of laser-switches for bus configuration and repair, and for overwriting static configuration signals are proposed.

1 Introduction

It is well known that the laser processing of integrated circuits is a powerful method to increase the yield and to configure chips. Various methods and devices were developed to process metallic connections and disconnections in microelectronic circuits. Recent investigations have focused on make-link technologies for two vertically or laterally adjacent metal lines. Several structures and processing methods have been shown for these technologies by Bernstein et al. [1,2], Hartmann and Hillmann-Ruge [3,4,5], and Chapman [6]. Break-link technologies have been used for several years ,e.g. in DRAM fabrication [7].

However, the problems of linking and cutting and the development of appropriate layout structures have been considered only separately. If complex repair or reconfiguration is the goal, two different devices had to be implemented for linking and cutting. Each of the devices requires its own area on the chip, increasing the total area of conventional laser structures.

Another important limitation is the long processing time required to access two separate devices, since a significant amount of time is needed to reposition the chip in the laser configuration system.

A main application for the combination of laser-links and fuses is to repair interconnects or bus systems in complex VLSI circuits. Although the feature size is going to decrease steadily over the next generations of VLSI circuits, it is predicted in the SIA Roadmap [8] that the effective length of bus lines or interconnects connecting different modules will stay constant or will even increase. In [9], bus repair using linking and cutting structures has been employed for yield enhancement of a multiprocessor chip with nine identical video processors for real time video coding. The Large Area Integrated Circuit (LAIC) of 16.6 cm² (manufactured in a 0.8 µm CMOS-Technology) comprised defect tolerant lines in global bus systems. The Application of laser configuration techniques lead to a yield increase of 13.3% [9]. The next-generation implementation of a multiprocessor video coding system will utilize 0.25-µm technology, allowing the integration of at least a tenfold increase in the number of transistors from that in [9]. Thus, application and development of redundancy techniques are crucial for the successful production of these LAICs. For the next multiprocessor chip, which will be fabricated this year, the laser configurable redundancy technique is used again. A result of this research is a multifunctional laser linking and cutting structure for microelectronic circuits.

The reminder of this paper is organized as follows. In Section 2, the principle of the laser-switch structure and the experimental setup is described. In Section 3, the experimental results are presented and discussed. Section 4, informs of the fault tolerance of laser-switches with respect to energy fluctuations. A preview of accelerated life-time tests is given in Section 5. The implementation of laser-switches in LAIC's is discussed in Section 6. Section 7 concludes the paper.

2 Experimental

2.1 Switch structure

A special test chip has been designed and fabricated in a standard six-level metal 0.25 µm CMOS process. Several different shaped laser-switches were manufactured. All structures use only the upper three metal layers (metal 4,5,6). In general, the laser-switches can be described as follows :

All laser-switches (Figure 1) consist of three stacked metal lines. Metal *n* and metal *n*+1 are connected to each other using a standard via of 0.4x0.4 µm². The width of the interconnect line in metal *n* is 1 µm. Metal *n*+1 and metal *n*+2 are widened and overlap to allow reliable laser positioning. The lateral dimensions of the test structures amount to 12x12 µm² and 10x10 µm². The integrated vias correspond to the minimum design rules (0.4x0.4 µm²) of the used 0.25 µm CMOS technology. To check out the influence of passivation, some sets of samples were depassivated. A nitride window is placed in the center of the test structures. Corresponding to the lateral dimensions of the laser-switches, the nitride windows were dimensioned. The depassivated area of a 12x12 µm² laser-switch is selected to 8x8 µm² and a 6x6 µm² window is placed on 10x10 µm² laser-switches. The test structures are organized in chains of ten to allow life-time tests. Due to layout

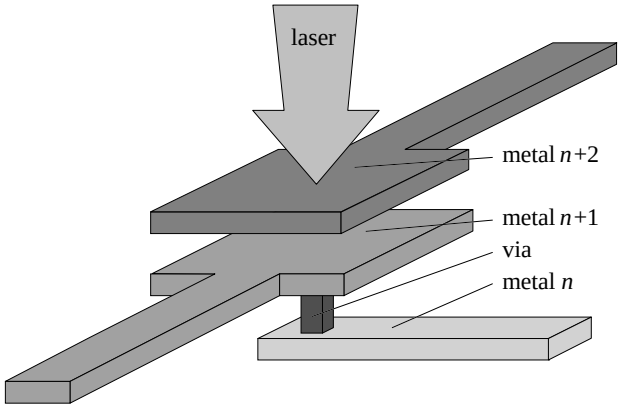

Figure 1 : Schematic of a laser-switch

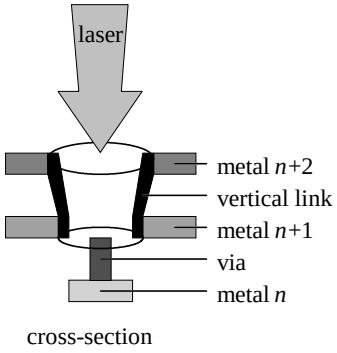

Figure 2 : Cross-section of a processed laser-switch

restrictions of the test chip, the implementation of longer chains was impossible. Furthermore, every interconnect line of the laser-switches is connected to a probe pad, to permit voltage and current measurements in order to determine the corresponding resistance.

The processing of the laser-switches is performed with a sequence of three laser pulses. The first pulse removes the passivation (and partially metal *n*+2). The second pulse eliminates metal *n*+2 completely. Metal *n*+1 is still covered with SiO_2 at this point. The last process step forms the ohmic contact from metal *n*+1 to metal *n*+2 and removes the link between via and metal *n*+1 (Figure 2). The vertical link to metal *n*+2 is built by vaporized and molten aluminum from the metal *n*+1 layer. To disconnect the via from metal *n*+1, metal *n*+1 has to be removed (vaporized) completely in the laser spot area, leading to a free standing via. It has to be ensured that the other process layer are not affected by the laser processing. To allow highly reliable processing of the proposed laser-switches, the melting points of the interconnect and via materials have to be taken into account. The tungsten via has a melting temperature of 3410 °C, while the melting temperature of the (aluminum based) metal lines is approximately 700 °C. Utilizing the correct energy dosis, the metal in layer *n*+1 is removed completely without corrupting the via and the underlying process layers.

2.2 Equipment

The experiments were performed on an automatic laser reconfiguration system which employs a excimer laser (max. rep. rate 200 Hz, XeCl, 308 nm, pulse duration 20 ns). The rectangular shaped beam of the excimer laser is collimated 1:2 by a Gallilei-telescope, directed by two mirrors and then truncated by an adjustable aperture. This aperture is projected through a displaceable lens arrangement on the back focal plane of a 36x reflecting objective (NA = 0.5) and finally focused on the test structures. The position of the samples under the objective is changed by a motorized XYZ-translation stage. The position accuracy of the motion system is ±0.5 µm with respect to xy-axis and ±0.1 µm with respect to the z-axis. An image processing system controls the precise position of the laser switches beneath the objective. The most important module of the laser configuration system is the energy monitor which controls precisely the energy dose of every pulse. The energy monitor co-operates closely with the software, in order to keep the total energy of a laser processing sequence constant.

3 Results

Based on our previous work [10] on laser-switches, we concentrated on optimal (minimal) structure sizes and most suitable laser parameters to process the structures. The previous investigations, performed with a small set of samples in a 0.5 µm CMOS-Technology have provided very good results, and the current work concerns the improvement of the laser-switch structure and the adaptation to 0.25 µm technology.

More than 300 laser-switches have been processed with the laser. A large part of the experiments was used to determine the optimal parameters to process this layer sequence. Values for optimal laser spot size, energy dose and number of pulses were determined. The determined parameters of 12x12 µm² laser-switches served as basis for processing of all further laser-switch structures. If necessary these parameters were modified and adapted for structure sizes of 10x10 µm². Table 1 gives an overview of the obtained results.

Table 1 : Resistance of the different laser-switch structures

Structure	R_{median} [Ω]	R_{min} [Ω]	R_{max} [Ω]
10x10 µm²	0.118	0.034	0.491
10x10 µm² depass.	0.527	0.272	1.421
12x12 µm²	0.065	0.009	0.368
12x12 µm² depass.	0.214	0.033	0.598

3.1 12x12 µm² laser-switch

Two different 12x12 µm² laser-switch structures were investigated. To check the influence of passivation for the process reliability, passivated and depassivated samples were designed, fabricated and examined. A 6.5x6.5 µm² laser spot was selected to process the 12x12 µm² laser-switches. The used energy ranges from 8 µJ to 12 µJ. These values are the summarized energy doses of a sequence of three single laser pulses with a energy density of 6 - 9 J/cm². Figure 3 shows the measured resistance depending on the laser energy. It can be clearly seen that the resistance of the processed laser links is very low.

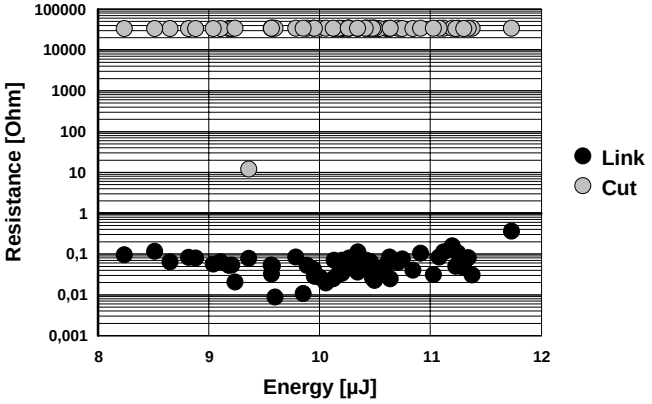

Figure 3 : Resistance versus laser energy of passivated 12x12 µm² laser-switches with a 0.4x0.4 µm² via

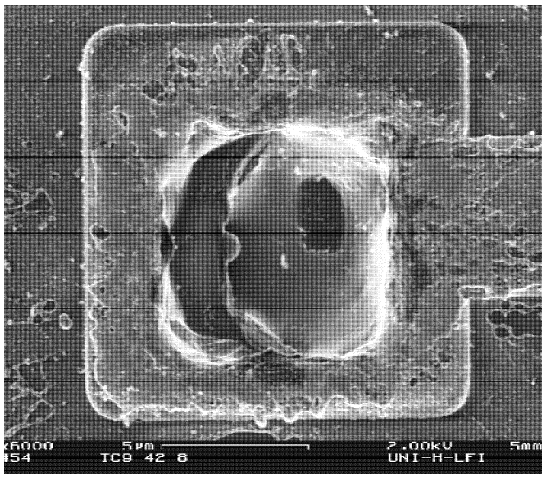

Figure 4 : REM image of an incorrect processed laser-switch

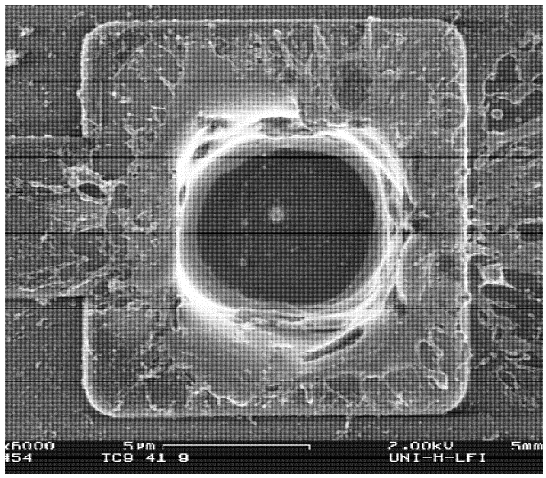

Figure 5 : REM image of a correct processed laser-switch

One laser-switch could not be successfully processed. The analysis of an REM image (Figure 4) of this laser-switch shows the reason for this malfunction. Because of a too low energy dose, metal *n*+1 could not be completely removed. Metal *n*+1 is still connected with the via by residuals of metal *n*+1. Thus, reliable processing is obtainable by increasing the energy. Energy doses of more than 9.5 µJ allow the processing of laser-switches with high reliability. The energy density of a single laser pulse has to be higher than 7.5 J/cm². A correctly processed laser-switch (Figure 5) shows a free standing via in the center and a completely removed metal *n*+1 layer in the laser spot area. The resistance of the formed links is very low (R_{medium}= 0.065 Ω) and an experimental yield of 100% is achieved by using three laser pulses with an energy density above 7.5 J/cm². Due to the missing passivation of the depassivated 12x12 µm² laser-switches, a lower energy dose (Figure 6) is necessary to process the structures. The generation of a burst pressure below the passivation, is not necessary anymore. Depassivated 12x12 µm² laser-switches are processable by a energy density of 5.5 J/cm². For both test structures similar electrical properties were determined. Best values for resistance (Table 1) could be observed at the passivated 12x12 µm² laser-switches. The increased resistance of the depassivated structures refers to a energy dose which was selected too high. Obviously, a large part of metal *n*+1 was totally

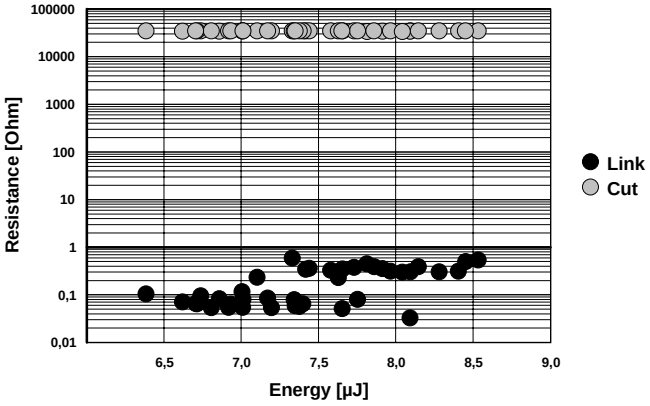

Figure 6 : Resistance versus laser energy of depassivated 12x12 µm² laser-switches with a 0.4x0.4 µm² via

vaporized. To obtain low values of link resistances, it is important to minimize the material loss by vaporization of metal *n*+1.

3.2 10x10 µm² laser-switch

Processing of the passivated and depassivated 10x10 µm² laser-switches is performed in the same way as the corresponding 12x12 µm² laser-switches, only the size laser spot was changed. The selected dimensions of the laser spot are 5.5x5.5 µm² with an energy density interval of 5 - 9.5 J/cm². The behavior of the passivated and the depassivated structures resemble that of the 12x12 µm² laser-switches. Processed passivated laser-switches (R_{median} = 0.118 Ω) show a less resistance as depassivated structures (R_{median} = 0.527 Ω). The reliability of 10x10 µm² laser-switches is comparable to 12x12 µm² laser-switches, only the resistance is slightly higher. The most important advantage of 10x10 µm² laser-switches is the area reduction of 30% compared to 12x12 µm² structures.

4 Energy tolerant behavior

Furthermore, an interesting effect could be observed after processing these structures. Several depassivated structures were exposed a too high energy dose. The condition that no other layer with exception of layer *n*+1 and layer *n*+2 should be affected by laser was violated. From experience it would be probable that the risk of short circuits up to metal *n*+1 rises. However, it seems that the modified laser-switch structures are more fault tolerant than samples of previous work. Mainly, the structures differ in via size and metal *n* interconnect width. The line width of metal *n*, which is connected with via was decreased from 4 µm to 1 µm. Also the via was shrunk to 0.4x0.4 µm². Figure 7 shows an REM image of a depassivated 12x12 µm² laser-switch which was processed by a too high energy dose. The vertical line in the center of the image represent the affected metal layer *n*. However, the quantity of material is not large enough to recreate a conducting connection between metal *n* and metal *n*+1. Metal *n* is completely vaporized and ablated. An undesired reconnection is excluded.

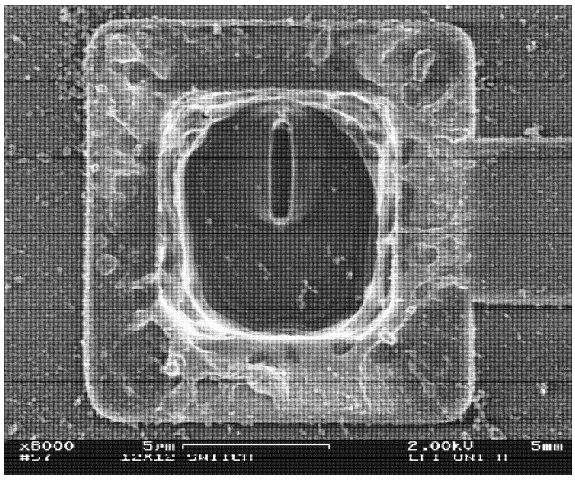

Figure 7 : REM image of a processed 12x12 µm² laser-switch. Metal *n* was affected by the laser processing

5 Accelerated life-time test

For a first estimation of life-time, a small set of samples were stressed. Test parameters were a substrate temperature of 230-250°C and a current of 60 mA. This corresponds to a current density of 1.5 A/cm² in the interconnect lines. Due to the unknown conducting profile of the link structure, statements of current density in the laser-switches are impossible. Assuming Black's equation, $t_{0.1}$ is approximately 22 years for expected operation conditions of 100°C and a current of 2.5 mA.

6 Implementation of laser-switches

In defect-tolerant designs, typical measures for yield improvement are bus configuration and activation, respectively deactivation, of redundant or multiple-count components. Conventional repair approaches are compared to a new approach, based on the laser-switches discussed before. The maximum length of the bus systems discussed here is 6 cm, and the bus systems contain up to 100 parallel signal lines. This large amount of dense uninterrupted interconnect area is particularly susceptible to defects. For this reason, laser-switches have been developed for yield enhancement purposes. Figure 8a shows an approach of bus line reconfiguration using traditional laser links and laser fuses, while Figure 8b represents the implementation and repair facilities of a bus system using laser-switches.

In both approaches (Figure 8a-b), interconnect level metal *n*+2 is utilized for spare lines. The primary bus lines are designed in the metal *n*+1 layer in Figure 8a, and in metal *n* in Figure 8b. Figure 8a depicts the repair approach used in [9]. Two laser links and four laser fuses have to be processed, to repair a defective bus line. In the first step, the defective bus

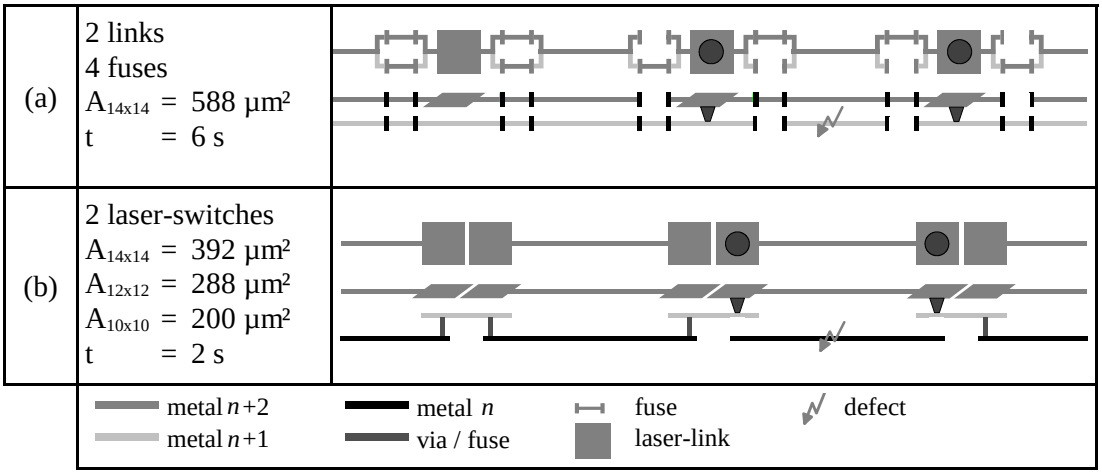

Figure 8 : Schematics of defect tolerant bus systems

line has to be resected from the primary bus by processing two laser fuses. Next, the defect is bypassed using two processed laser links. In a last process step, the part of the spare line which is used for bypassing, has to be disconnected from the rest of the spare line by processing two laser fuses. The overall positioning and processing time for this approach is around six seconds. The required processing time depends on the route length, the speed of

the translation stage, and the performance of the image processing system. However, the above processing time serves as a benchmark for the processing time of the proposed bus system using laser-switches. The pure laser processing time is less than 0.5 s. If laser-switches are utilized for bus system repair, the number of processing steps can be reduced (in addition to the reduced area overhead of this structure). Figure 8b shows a schematic view of the proposed laser-switch structure. Only two laser-switches have to be processed to perform the complete repair (i.e., bypassing the defective part of a bus line). Compared to [8], this new approach reduces the processing time per bus defect by 66%, in addition to reducing the area overhead for the laser structure by 33%. In this example the lateral dimensions of the link structure are equal. If the minimized laser-switches of 10x10 µm² are implemented, an area reduction of 65% is possible.

These results were calculated. Due to layout restrictions, routing overhead and route length the application of 14x14 µm² laser-switches in real layouts reduces the area only by 20% and the time only by 50%. A careful estimation for configuration arrays of 10x10 µm² laser-switches shows that an area reduction of 30-35% could be achieved. This has to be proved by designing a real layout.

Another interesting application is the implementation of laser-switches for fault tolerance in static configuration circuits. For LAIC's containing several subsystems, it is essential to identify each subsystem by static configuration signals. A corrupted signal causes a malfunction of the LAIC. The outputs (Figure 9, output c) of the logic devices which generate the identity signal can be overwritten by laser processing of a laser-switch arrangement (Figure 9).

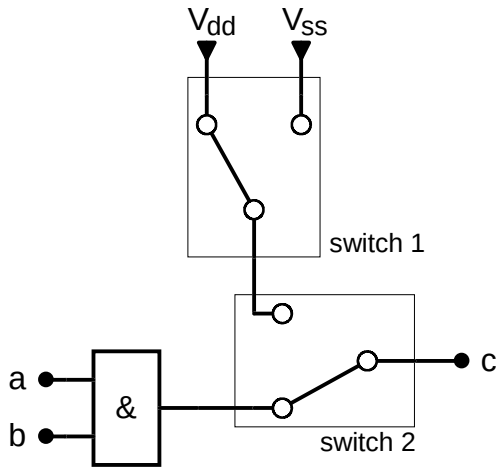

Figure 9 : Laser-switch arrangement to overwrite static configuration signals

7 Conclusions

In this paper, we presented a device and some methods for yield enhancement of Large Area Integrated Circuits. The redesigned and improved laser-switch structure reduces the area by 30% and the processing time up to 50% compared to previous work [8]. Test structures have been fabricated in a standard six-level metal 0.25 µm CMOS process and have been successfully verified. They were processed with very high yield and excellent

electrically properties. The experiments have shown fault tolerance with respect to energy fluctuations. In particular, the 10x10 µm² laser-switch is well-suited for repair and reconfiguration purposes in VLSI circuits.

Acknowledgments

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