Signal Integrity Problems in Deep Submicron arising from Interconnects between Cores

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Abstract

The SIA Roadmap shows a very aggressive drive to deep submicron designs. A significant corner stone in the industries' ability to utilize this tremendous capabilities is the usage of reusable cores. When employing cores, one must be sensitive to the quality of the interconnects which will carry signals between cores and the ASIC portion of the network. In this work we will use an extremely accurate line simulator which solves the transmission line equations derived from Maxwell's equations for the simulation of line systems. We will show that the coupling between bus lines is significant, since the signal delay can be increased and even hazards can occur. Furthermore, these effects depend on the set of input signals of all bus lines and the skew between the individual input signals. The lines' cross sections are taken from the SIA Roadmap going from 0.35 µm technology design down to 0.10 µm technology design.

1 Introduction

The SIA Roadmap [1,2] predicts a very aggressive path of technologies from 0.35 µm technology design to 0.10 µm technology design and beyond. As a result, ASICs will have 5M gates per chip in 0.35 µm technology going to 430M gates per chip in 0.10 µm technology. With this tremendous capacity it is possible to start very serious utilization of reuseable cores. From a business point of view this creates an advantage since one can get to the market faster with a higher assurance that these core functions have far fewer intrinsic design errors relative to a raw new design. In addition, this approach will greatly increase the productivity of the design community. With this new direction comes a number of issues which need to be examined. Testing is clearly one main issue and this has given birth to the proposed IEEE Standard P1500 activity to address this. Another area of concern is that of signal integrity of the interconnects which bind these cores to one another and to the ASIC portion of the network. The analysis of these line systems is the subject of this work.

The interconnects must not only be analyzed with regard to opens and shorts but also with regard to the signal delays. It has to be considered that the signal delay (i.e. the time between the moments when the signal crosses the mid-voltage point at the input and output) on a certain line within a bus system depends on the set of input signals of all bus lines. Different sets of input signals lead to minimum and maximum delays which are strong functions of coupling. Additionally, hazards can occur.

For the analysis of the line systems we will use an analog simulator which solves the transmission line equations derived from Maxwell's equations in the time domain. For this reason, the resulting model takes into account wave propagation effects and consequently the results are very accurate. This model does not only consider the capacitive coupling between all bus lines, it will also include all self and mutual inductance effects. Some researchers are pointing to the ever increasing importance of self and mutual inductances in the line system [3,4,5,6]. Furthermore, the

solution of the transmission line equations results in a simulation algorithm which does not require matrix inversion or convolution so that the algorithm is very efficient and stable.

In section 2, the line model will be presented. In section 3, we will give the technology specific parameters extracted from the SIA Roadmap. They are based on metal level 5, which is suited best for busses since it displays the lowest resistivity. In the following section 4, the simulation results of different 9-line systems are presented. We will finish in section 5 with the conclusions.

2 Line Simulation

Starting from Maxwell's equations one can derive the transmission line equations (1a,b) describing the currents and voltages propagating on lossy coupled multiconductor transmission lines.

$$\frac{\partial \underline{V}(x,t)}{\partial x} = -\left(\mathbf{R}' + \mathbf{L}'\frac{\partial}{\partial t}\right)\underline{I}(x,t)$$
$$\frac{\partial \underline{I}(x,t)}{\partial x} = -\left(\mathbf{G}' + \mathbf{C}'\frac{\partial}{\partial t}\right)\underline{V}(x,t) \qquad (1a,b)$$

Herein $\underline{V}$ and $\underline{I}$ represent the column matrices of line voltages and currents along the lines at location x (coordinate of the line length). **L'**, **C'**, **R'** and **G'** represent the square matrices of the per unit length inductances, capacitances, resistances and admittances of the line system. The transmission line equations (1a,b) are sets of partial coupled differential equations. In contrast to ordinary differential equations they are able to describe wave propagation effects. These effects are, first, the finite transmission time that a signal needs to propagate from the input to the output, second, reflections due to mismatched line terminations, third, dispersion which results from the fact that the propagation velocity is a function of frequency and fourth, electromagnetic coupling between the lines. All this ultimately leads to the delay of the signals, to noise and to multiple switching effects (hazards).

The time domain solution of (1a,b) leads to a so called distributed model. This model results directly from the transmission line equations and therefore takes into account the wave propagation effects. Herewith, a lossless line is modelled exactly by only one lossless segment representing the closed form solution of the transmission line equations for the lossless case. Since an analytical solution for lossy line systems is not known, the lossy lines are divided into a small number of segments in the direction of the wave propagation. Each segment except the last one consists of a lossless line system together with an attenuation network as shown in Fig. 1.

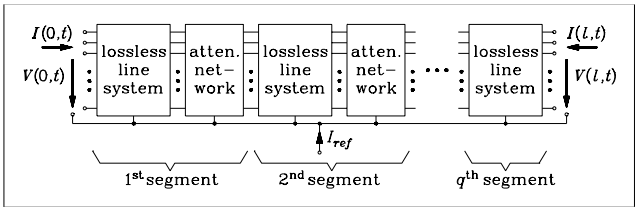

Fig. 1 Distributed model of lossy coupled lines

In detail, the lossless line system and the attenuation network are modelled as shown in Fig. 2. The voltage sources $V_1^k(t)$ represent the waves travelling to the right whereas the voltage sources $V_2^k(t)$ contain the values of the leftward travelling waves. T^k is the transmission time per segment and Z_0 represents the characteristic impedances. The model together with an algorithm for the simulation in the time domain is described in detail in [7].

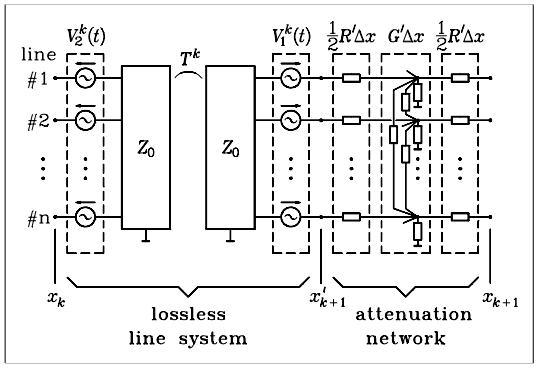

Fig. 2 Physical model

This transmission line model has been integrated into a SPICE-like circuit simulator [8]. For the analysis of the line system no numerical integration is needed. This leads to a very fast and stable algorithm. Since this model is based on the exact solution of the partial differential equations the results are very accurate. This tool has been used for the investigations presented in section 4.

3 SIA - Roadmap

With the help of a sample geometry with five metal layers as shown in Fig. 3 we examined how scaling in deep submicron affects the quality of signals. The geometric data

for the different technologies has been derived or extracted directly from the SIA Roadmap (see Tab. 1).

technology		0.35µ	0.25µ	0.18µ	0.13µ	0.10µ
w5	µm	≥0.8	≥0.6	≥0.44	≥0.3	≥0.22
s5	µm	≥2.0	≥1.5	≥1.1	≥0.75	≥0.55
h5	µm	1.2	1.2	1.1	0.9	0.77
d	µm	7.9	7.9	7.2	6.0	5.6
epitaxy	µm	3.0	2.0	1.4	1.0	0.8
substrate	µm	400	400	400	400	400
frequency	Mhz	333	500	666	900	1100
V_{DD}	V	3.3	2.5	1.5	1.35	1.2

Tab. 1 Geometry data from SIA Roadmap

In the first step, we extracted the transmission line parameters (resistance, inductance, capacitance and admittance per unit-length) using a tool developed in our institute [9] which is based on two-dimensional quasi-analytical formulae while the cross-sectional geometry is assumed to be homogeneous along the lines. For random samples, the results have been verified with the help of a commercial finite-element field calculation program. All cross-sectional information about a particular line system (material, geometry, return-path of the current) is contained in these per-unit-length parameters.

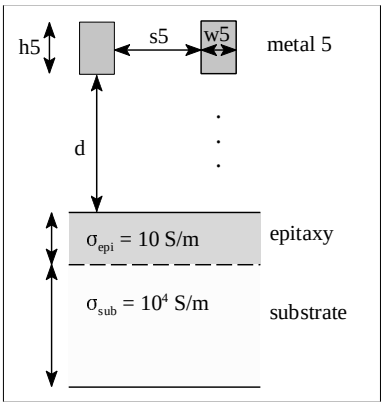

Fig. 3 Sample geometry

In the second step, we simulated different line systems with different load capacitances for the technologies given in Tab. 1 for four different sets of input signals. In the first case, the signal on middle line changes while all other lines are fixed to ground. This case yields the intrinsic delay. In the second case, all lines switch in the same direction which is called the even mode. In the third case, the outside lines change from low to high while the middle line changes from high to low (or vice versa). This is refered to as the odd mode. In the fourth case, the middle line is quiescent while the outer lines switch. Fig. 4 shows the setup for a 9-line-system for which the simulation results are given in the following section. The simulations have been performed with the tool mentioned above which uses the distributed line model described in the previous section. Our investigations focus on long bus systems. Therefore, as a representative circuit, a 9-line system has been chosen because further simulations demonstrated that the coupling between lines that are not direct is not negligible. The driver resistances are Z_D = 50 Ohm since we focused on long lines which require strong drivers, and the output capacitances decrease from C_L = 0.05 pF for 0.35 µm technology to C_L = 0.01 pF for 0.10 µm technology.

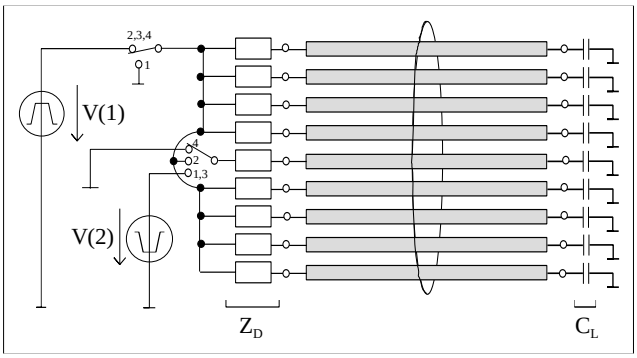

Fig. 4 Simul. circuit with different sets of input signals

4 Line Simulation Results

In this section, we examine the effects of signals propagating along a 9-line system located in metal 5 which shows the lowest resistivity. Tab. 2 gives some of the line parameters which have been used. Notice, that the coupling capacitance C'_{56} which is the capacitance of line 5 to its neigbour line 6 increases dramatically as we approach 0.10 µm technology. It is almost double that of 0.35 µm technology. This is a direct result of smaller design rules which allow the lines to move closer together. In contrast, the inductance does not vary much with changes in the geometry from one technology to another. This slow change with respect to the technology is due to the fact that the inductance varies in a logarithmic way. Finally, the line resistance is

	0.35µm	0.25µm	0.18µm	0.13µm	0.10µm
C'_{56} in pF/m	41,59	49,73	56,93	64,17	70,54
C'_{55} in pF/m	12,89	10,06	9,65	7,30	6,42
L'_{12} in µH/m	0,80	0,84	0,88	0,93	0,97
L'_{11} in µH/m	1,17	1,17	1,18	1,21	1,23
R' in kΩ/m	36	50	74	133	210

Tab. 2 Line parameters for metal 5

shown to increase from 36 kΩ/m for 0.35 μm technology to 210 kΩ/m for 0.10 μm technology.

The interconnects have been analyzed in view of the signal delay. The delay of a certain line within a bus system depends on the set of input signals of all bus lines. The signal travels on a line with its intrinsic delay when only this certain line is switched and all the other lines are quiescent which is refered to as case 1 in Fig. 4. The intrinsic delay is used as a reference. Driving the line system in even mode leads to a minimum signal delay (shorter than the intrinsic delay) whereas driving it in odd mode results in a maximum signal delay which can be much longer than the intrinsic delay. The Figs. 5 and 6 illustrate the dependency of the signal delay from the set of input signals. (It is assumed that there is no skew between the individual input signals.)

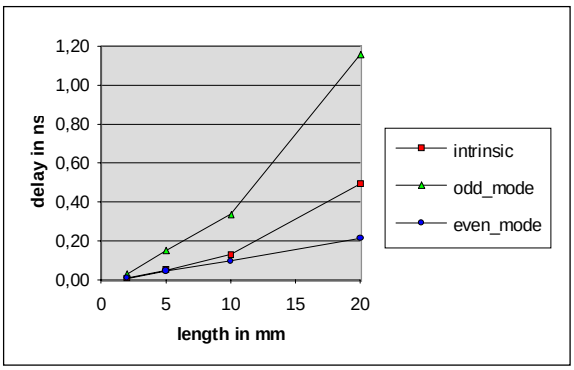

Fig. 5 Signal delay for different sets of input signals in 0.35 µm technology

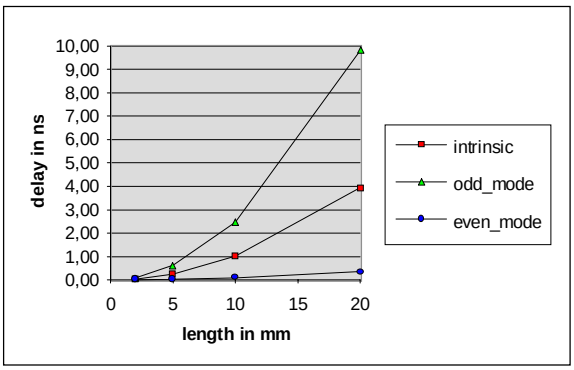

Fig. 6 Signal delay for different sets of input signals in 0.10 µm technology

Furthermore, we have done a number of simulations for odd mode driven line systems with the center line changing within a realistic tolerance earlier and later relative to the outside eight lines, i.e. the falling edge of the middle line occurs within 500 ps earlier (negative skew) or later (positive skew) than the rising edges of the outer lines. Thus, when the skew is negative then the signal on the center line has already started falling to zero so that the coupled noise from the outer lines occurs during or after the falling edge and therefore raises again the signal on the center line. This can lead to a dramatic increase in the signal delay and even hazards can be created. The increase in signal delay and the occurrence of hazards depend on the skew between the individual input lines. These effects are mainly caused by the electromagnetic coupling between the lines. They are demonstrated in Fig. 7 to 10 for 2 mm and 10 mm long 9-line systems in 0.35 μm and 0.10 μm technology.

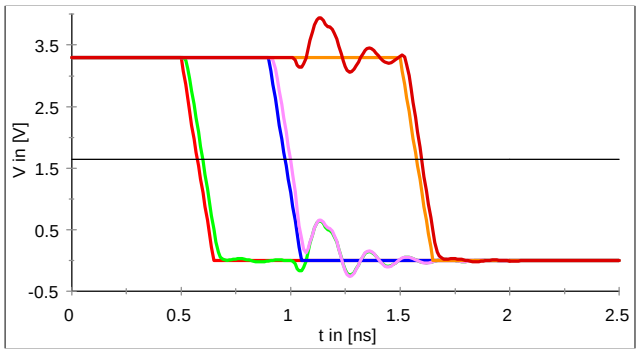

Fig. 7 Signal delay of a 2 mm long 9-line system in 0.35 µm technology for different skew (-500 ps, -100 ps, +500 ps)

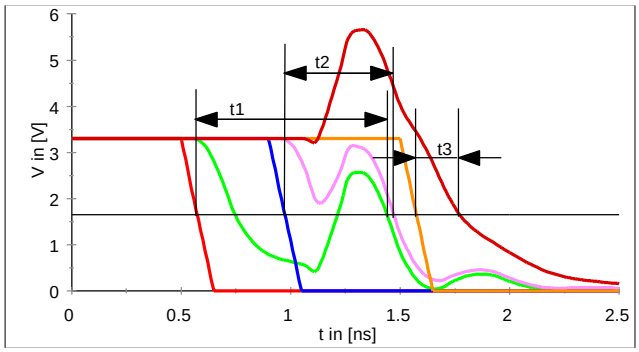

Fig. 8 Signal delay (t1, t2, t3) of a 10 mm long 9-line system in 0.35 µm technology for different skew (-500 ps, -100 ps, +500 ps)

For a 2 mm line system in the 0.35 μm technology the outer lines couple a signal onto the middle line but the signal delay is only slightly affected (see Fig. 7). This is different for the 10 mm line as can be seen in Fig. 8. Here, the

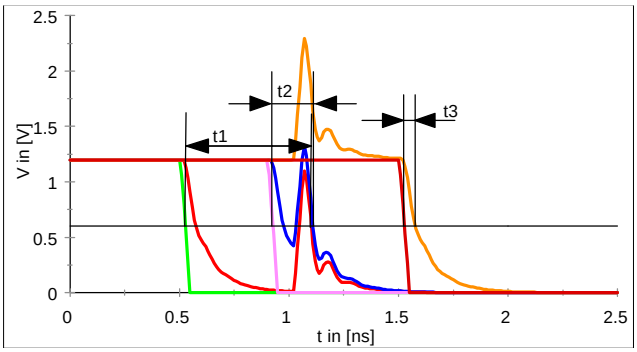

Fig. 9 Signal delay (t1, t2, t3) of a 2mm long 9-line system in 0.10 µm technology for different skew (-500 ps, -100 ps, +500 ps)

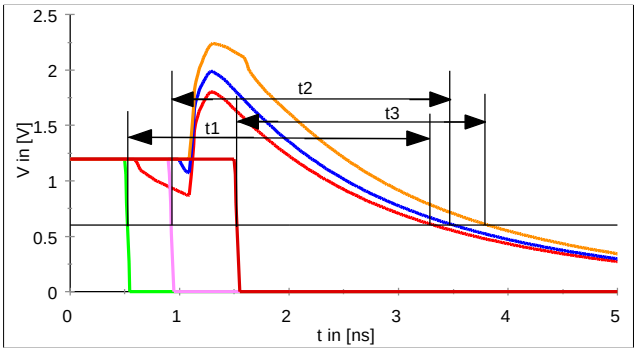

Fig. 10 Signal delay (t1, t2, t3) of a 10 mm long 9-line system in 0.10 µm technology for different skew (-500 ps, -100 ps, +500 ps)

induced signal is so large that the threshold (assumed to be the mid-voltage point) is crossed three times which results in a hazard, if the falling edge occurs earlier than about 100 ps before the rising edges of the outer lines. But independently from the appearance of hazards the signal delay is increased dramatically due to the coupling between the lines.

When scaling down technology, these effects become stronger and already shorter lines are significantly affected in signal delay and are susceptible to hazards as is shown for example in Fig. 9 for a 2 mm long 9-line system in 0.10 μm technology. Already on a 2 mm long line system hazards can occur and the signal delay is increased (see Fig. 9). For the 10 mm line, hazards no longer occur but the signal delay is increased drastically (see Fig. 10). Thus, if these nine lines are used as a bus system and they are clokked at the end of the line into a register this can cause incorrect data when the clock arrives too early or within a hazard. Finally, if this center line was a clock line, a totally none functioning signal would result in incorrect operation.

Finally, we investigated how quiescent lines are affected by coupling. The simulated circuit corresponds to case 4 in Fig. 4 where the middle line remains quiescent while the outer lines are all switching in the same direction. For 0.35 μm technology the induced voltage on the 2 mm passive line remains small enough and does not cross the mid voltage point (see Fig. 11). But going down in technology, the capacitive coupling increases and hazards begin to appear as is shown in Fig. 12. The occurence of hazards is not due to the shorter rise time of the input signal with scaled down technology because the effect is dominated by the electrical coupling. The effect becomes stronger with increasing ratio of coupling capacitance to ground capacitance.

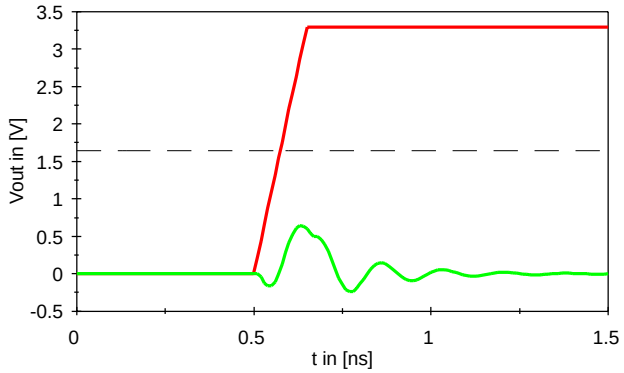

Fig. 11 Output voltage of the quiescent center line of a 2 mm long 9-line system in 0.35 µm technology

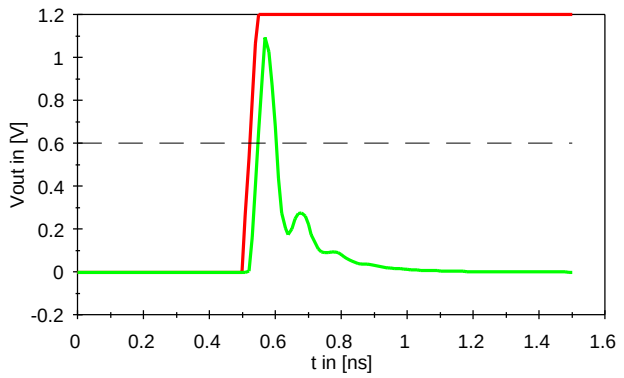

Fig. 12 Output voltage of the quiescent center line of a 2 mm long 9-line system in 0.10 µm technology

The simulation results presented above demonstrate that the coupling between lines has strong influence on the signal delay which depends on the set input signals and the skew between them. Additionally, hazards can occur on switching as well as on quiescent lines. Consequently, the

interconnects have to be taken into account not only within design and validation but also within testing. More complex delay tests have to be developed which take into consideration coupling effects and test pattern have to be generated which stimulate the worst delay.

5 Conclusions

It has been shown that much care has to be taken when interconnecting busses from one core to another core are designed. First, accurate simulation tools are needed to simulate the signal propagation along the line system accurately enough by considering coupling effects. As we go to more aggressive technologies we have to make sure that lines that travel together will not result in incorrect operation due to hazards and increased signal delays. Both, the appearance of hazards and the increase in signal delay depend strongly on the set of input signals of the line system and the skew between them. Therefore, the interconnects have to be taken into account within design, validation and testing.

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