Core Interconnect Testing Hazards

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The SIA Roadmap predicts a very aggressive path of technologies from 0.35 µm to 0.10 µm technology design. Increasing frequencies together with decreasing geometries lead to a number of issues which need to be examined. Testing is clearly one main issue. Another area of concern is that of signal integrity of the interconnects.

The interconnects must not only be analyzed with regard to opens and shorts but also with regard to the signal delays. In addition, it has to be considered that the signal delay (i.e. the time when the signal crosses the switching threshold of the following gate) on a certain line within a bus system depends on the set of input signals of all bus lines. Furthermore, hazards can occur. Both effects are due to coupling and can lead to an incorrect function of the whole circuit.

Different interconnect systems with different test pattern have been analyzed. The geometric data for the interconnects has been extracted from the SIA-Roadmap. Table 1 shows the geometric data for lines located in metal layer 5.

technol.	**0.35µ**	**0.25µ**	**0.18µ**	**0.13µ**	**0.10µ**
line width	≥0.8	≥0.6	≥0.44	≥0.3	≥0.22
spacing	≥2.0	≥1.5	≥1.1	≥0.75	≥0.55
line height	1.2	1.2	1.1	0.9	0.77
oxide	7.9	7.9	7.2	6.0	5.6
epitaxy	3.0	2.0	1.4	1.0	0.8
substrate	400	400	400	400	400
freq. Mhz	333	500	666	900	1100
V_{DD} V	3.3	2.5	1.5	1.35	1.2

Tab. 1 Geom. data (in µm) from SIA

First, the line parameters for the simulation of the interconnects have been calculated using a tool which takes into account conducting subtrates. It is based on two-dimensional quasi-analytical formulas.

Second, the line systems have been analysed with the help of a time-domain simulator for lossy coupled lines. It is based on the exact solution of the transmission line equation derived from Maxwell's equations and consequently takes into consideration wave propagation effects.

We examined the effects on signals propagating along a 9-line system located in metal 5 which is suited best for busses since it displays the lowest resistivity.

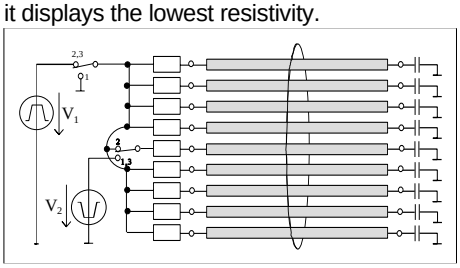

Fig. 1 9-line system driven in different modes

The interconnects have been analyzed in view of the signal delay. The signal travels on a line with its reference delay when only this certain line is switched and all the other lines are quiescent (switches in position 1 in figure 1). In the even mode all bus lines switch in the same direction (position 2) which may lead to a minimum delay (shorter than the reference delay) whereas in the odd mode the middle line switches against the outer eight lines (position 3) resulting in a maximum delay which can be much longer than the reference delay. Figure 2 illustrates the dependency of the signal delay from the set of input signals.

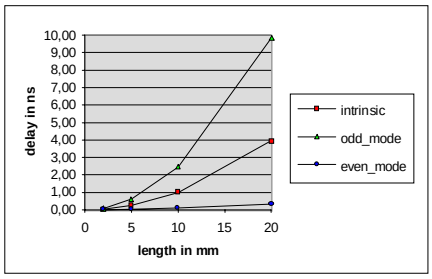

Fig. 2 Signal delay for different sets of input signals in 0.10 µm technology

Furthermore, we have done a number of simulations with odd mode input signals with the center line changing within realistic delays earlier and later relative to the outside eight lines, i.e. the falling edge of the middle line occurs within 500 ps earlier or later than the rising edges of the outer lines in order to determine the worst delay. The signals at the ends of the middle line of a 2 mm and a 10 mm line system are shown in figures 3 and 4.

For a 2 mm line system the signal delay is increased and hazards can occur depending on the skew between the individual input signals (see figure 3). For the 10 mm line, hazards no longer occur but the signal delay is increased drastically.

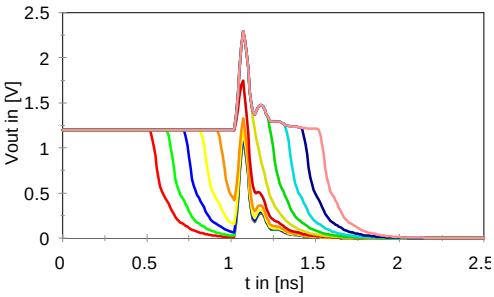

Fig. 3 Output voltage of the middle line of 2 mm odd mode driven 9-line system in 0.10 µm

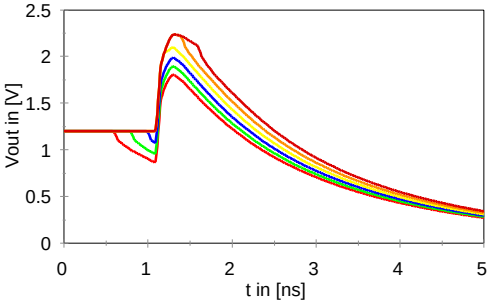

Fig. 4 Output voltage of the middle line of 10mm odd mode driven 9-line system in 0.10 µm

Both, the increase in signal delay as well as the occurence of hazards is due to the electromagnetic coupling between the interconnects.

By doing extremely accurate solutions to Maxwell's equations of line systems, one can see the strong impact on neighbouring lines. This results, in the best case, only in a wide difference between minimum and maximum delays. This difference can be as much as 20:1 for a 20 mm line in 0.10 µm technology. In the worst case, dynamic hazards can occur asyncronously and totally invalidate data on busses interconnecting cores. Clocks are particularly vulnerable as a result of the ability to change states of cores receiving them, if a hazard occurs. Thus, testing now must enter the world of solving wave equations to be certain of proper operation.

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