LFSR Test Pattern Crosstalk in Nanometer Technologies

Dieter Treytnar*, Michael Redeker†, Hartmut Grabinski and Faïez M. Ktata
Information Technology Laboratory, University of Hannover, Germany, dieter@lfi.uni-hannover.de

Abstract

In this paper we investigate the crosstalk influence of interconnects on test patterns in integrated circuits in today and future technologies. The test patterns are produced by a linear feedback shift register (LFSR). We show the per unit length line parameters L', C' and R' of interconnects in 150 nm down to 35 nm technologies wherefore we assume the smallest geometries predicted by the SIA roadmap. Using these parameters we demonstrate that crosstalk influences the signal behaviour depending on the technology used. The test patterns were generated by a 5 bit LFSR using an interconnect system with a length of 1 mm in these future technologies.

1 Introduction

The problem of testing in the nanometer age will become more important in the future because of increasing frequencies, decreasing geometries and decreasing voltages. The SIA Roadmap [1] predicts a very aggressive path of technologies from 150 nm to 35 nm technology design. As a result, integrated circuits consisting of 220M gates per chip in 150 nm technology will go to 20,000M gates per chip in 35 nm technology. Additionally, the frequency will increase from 1.4 GHz in 150 nm up to 8 GHz in 35 nm technology and simultaneously V_{dd} will decrease from 1.2 Volts down to 0.45 Volts. So, beside the question: 'How does scaling in nanomenter technologies affect the quality of signals on typical interconnects ?' it is also important to answer the question 'How stable are the test patterns against crosstalk ?'.

In previous works [6] we have shown the influence of switching signals on lines in submicron designs down to 100 nm technology and their influence on the adjacent signal lines due to crosstalk. In this work, we show the effects of test pattern crosstalk down to 35 nm technology.

For the analysis of the line systems we use an analog simulator which solves the transmission line equations derived from Maxwell's equations in the time domain [3, 4]. The resulting model takes into account all wave propagation effects.

2 Geometric Data and SIA-Parameters

Assuming a sample geometry with five copper metal layers we have examined how scaling in deep submicron affects the quality of signals. Based on such a geometry the geomtric data for different technologies was taken from the SIA roadmap. First, we extract the transmission line parameters (resistance, inductance and capacitance per unit-length) using an in-house tool [5] which is based on two-dimensional quasi-analytical formulas. For random samples, the results have been verified with the help of a commercial finite-element field calculation program as well as by measurements.

Tab. 1 shows the geometric data for the lines located in metal layer 5.

technology		150nm	100nm	70nm	50nm	35nm
width	μm	≥0.33	≥0.22	≥0.16	≥0.10	≥0.08
spacing	μm	≥0.81	≥0.55	≥0.39	≥0.26	≥0.20
heigth	μm	0.92	0.77	0.55	0.36	0.29
dist. to subst.	μm	6.54	5.735	4.725	3.87	3.345
epitaxy	μm	2.0	1.0	1.0	1.0	1.0
substrate	μm	400	400	400	400	400
frequency	Mhz	1400	2000	3000	5000	8000
V_{DD}	V	1.2	1.2	0.7	0.55	0.45

Table 1: Geometry Data from SIA Roadmap for Metal Layer 5

The line parameters presented in Fig. 1 to 5 are extracted from a 5 line system in SIA geometries for different metal layers. The corresponding line system is depicted in Fig. 8.

In detail, Fig. 1 shows the self capacitance per unit length of the center line of this 5 line system and Fig. 2 shows the mutual capacitance per unit length of line 3 and 4. The inductances per unit length are shown in Fig. 3 (self inductance) and Fig. 4 (mutual inductance), respectively. Finally, Fig. 5 shows the resistance per unit length.

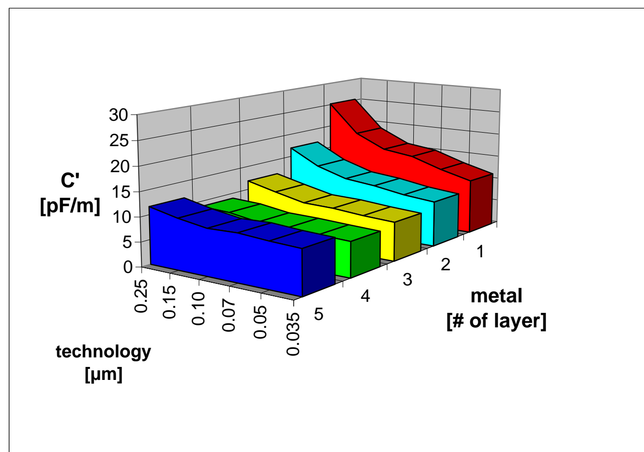

Figure 1: Self Capacitance extracted from SIA

*Dieter Treytnar is now with the edacentrum, Germany.

†Michael Redeker is currently visiting the University of Alberta, Dept. of Electrical and Computer Eng., Edmonton, Alberta, Canada.

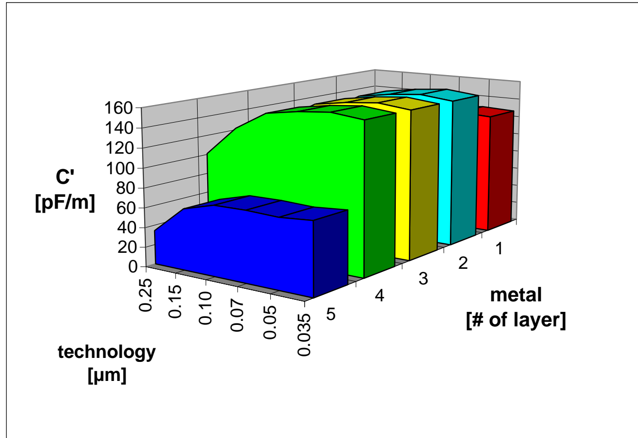

Figure 2: Mutual Capacitance extracted from SIA

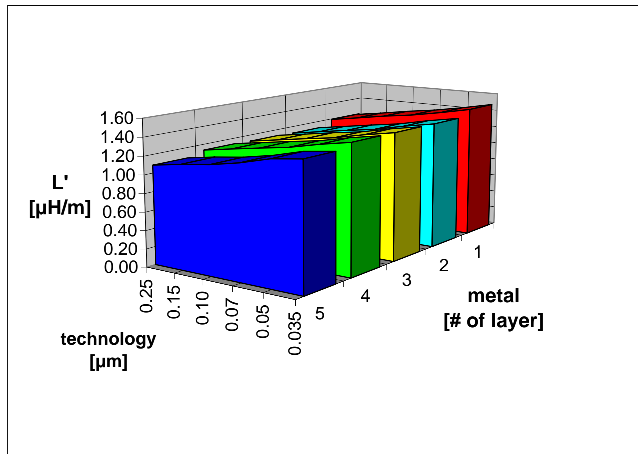

Figure 3: Self Inductance extracted from SIA

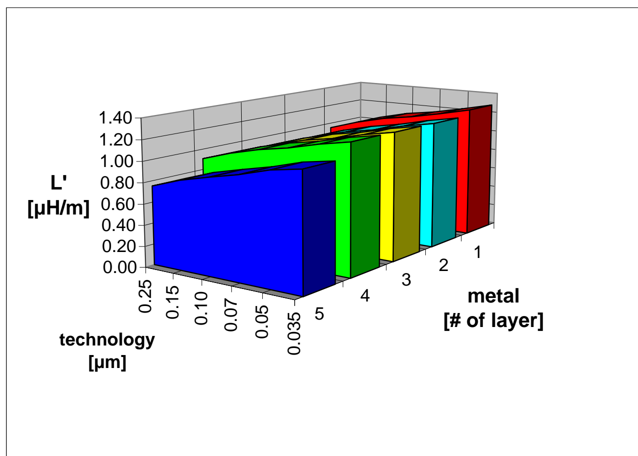

Figure 4: Mutual Inductance extracted from SIA

Due to the very small cross-section dimensions the resistance per unit length plays the most important role for the future. It increases from a few hundred kΩ up to 1 GΩ in metal 5 - and up to 3 GΩ in metal 1 (all per unit length). In contrast, the mutual capacitances are nearly constant in the smaller technologies in metal 5 and increase a little in the other metal layers. The inductances increase linearly in each metal layer for decreasing technology sizes.

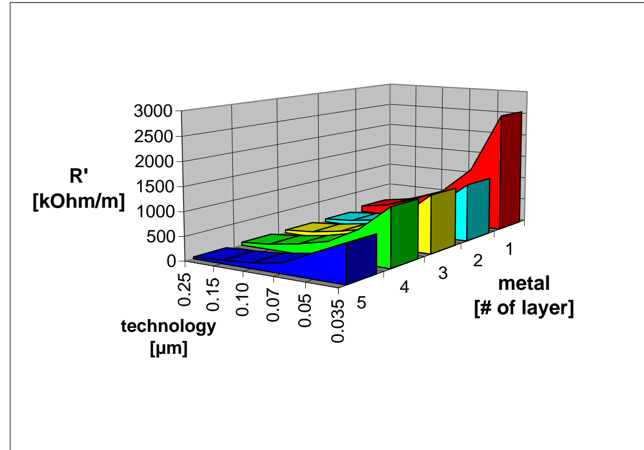

Figure 5: Resistance extracted from SIA

3 Linear Feedback Shift Register

As [7] stated, future integrated circuits will likely be tested by self test strategies only. The most common built-in test pattern generator used in today's chip designs is the linear feedback shift register (Fig. 6). An LFSR is a

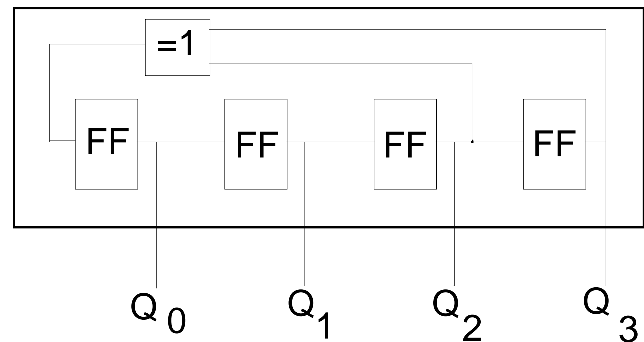

Figure 6: Linear Feedback Shift Register

shift register with feedback loops which performs polynomial divisions. By implementing the LFSR in such a way that the dividing polynomial is a primitive polynomial, the LFSR can generate all possible bit combinations but not the singular state where the LFSR is kept in one state (e.g., "000...000"). Thus an LFSR can adopt $2^n - 1$ states and can be described in a mathematical way straightforward [8]. Its easy implementation with small area overhead and its powerful properties of generating pseudo-random patterns make an LFSR so attractive for test pattern generation. Typically, the test pattern of an LFSR produces from time step to time step ones and zeros in such way that very strong crosstalk effects arise. The principle of shifting 0's (white squares) and 1's (black squares) is represented in Fig. 7.

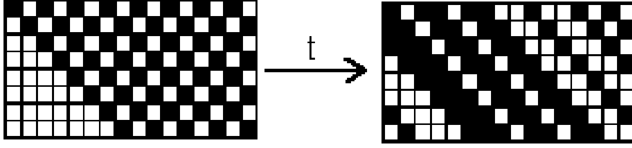

Figure 7: Test Pattern Structure of an LFSR

4 Simulation Results

Fig. 8 shows the setup for the 5-line-system under test. For the simulation, we have used the distributed line parameter model previously introduced. The driver resistances are assumed to $Z_D = 50\ \Omega$ each and the output capacitances decrease from $C_L = 20$ fF in 150 nm technology to $C_L = 3$ fF in 35 nm technology. In all cases the line length is 1 mm and the chosen line material is copper.

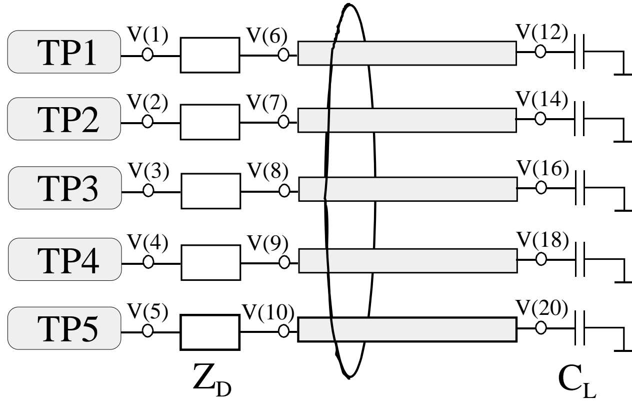

Figure 8: Simulated Circuit

The input of the line system is loaded by the digital test patterns of a 5 bit LFSR which are previously converted into 'analog' signals whereas the test pattern frequency is 1.4 GHz in 150 nm technology and 8 GHz in 35 nm technology. In Fig. 9 to Fig. 11 the 5 bit test patterns at the drivers output, at the beginning (near end) as well as at the end of the line system (far end) are depicted (each graph shows the first three lines only). The input signals are identified as V(1) to V(3), the signals at the near ends of the line as V(6) to V(8) and the output signals at the far ends of the line as V(12) to V(16) (cf. Fig. 8). V(10110) represents the digital threshold voltage $\frac{V_{dd}}{2}$.

Fig. 9 to 11 show the behaviors from 70 nm technology down to 35 nm technology. In 100 nm technology (not shown) the interference between the 5 lines is negligible and the line geometries are noncritical. Therefore in this case the test patterns of the LFSR will be transmitted to the end of the line fault free in the digital sense.

Some crosstalk effects can be observed in 70 nm technology (Fig. 9), but there are also no effects with respect to digital circuits.

The simulation in 50 nm (Fig. 10) shows stronger crosstalk effects which do not lead to faults in the digital world, but due to the higher resistances the propagation

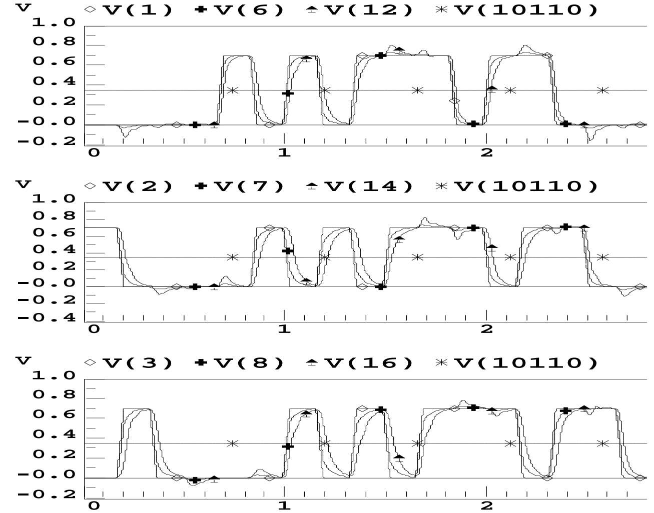

Figure 9: Near and Far End Signal in 70 nm Technology

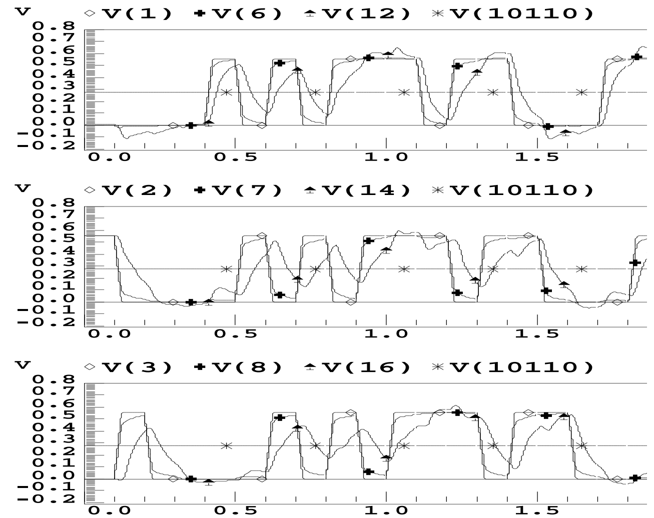

Figure 10: Near and Far End Signal in 50 nm Technology

behaviour will be dominated by delay effects.

Finally, in 35 nm technology (Fig. 11) the digital signals at the far end of the line are not fault free anymore. In this technology, the SIA roadmap predicts a clock frequency of more than 8 GHz. Due to the strongly increasing resistance (about 800 kΩ/m) an 8 GHz digital signal cannot be propagated error free for this line length: the signal will no more reach the threshold voltage ($\frac{V_{dd}}{2}$) between high (digital 1) and low (digital 0) level in some cases. The LFSR test patterns will be transmitted with errors only.

By comparison Fig. 12 shows the signals simulated without any inductive or capacitive coupling between the lines. Obviously, the output signal behaviour is strongly influenced not only by the line losses but also by coupling effects. For example, at t=0.5 ns there is a different digital signal in both graphs. A comparison with Fig. 11 shows

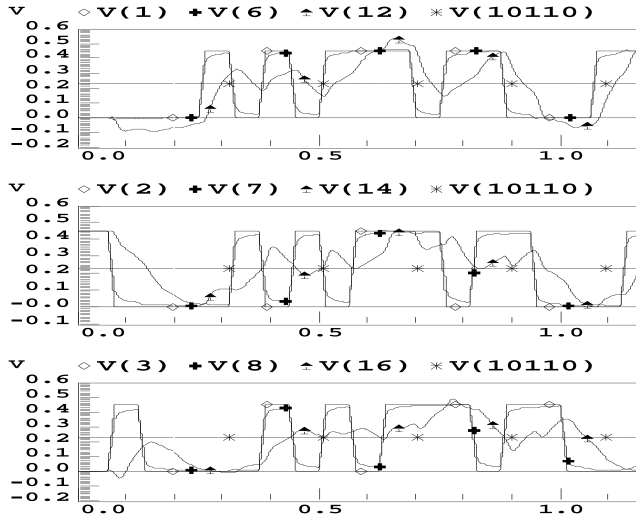

Figure 11: Near and Far End Signal in 35 nm Technology

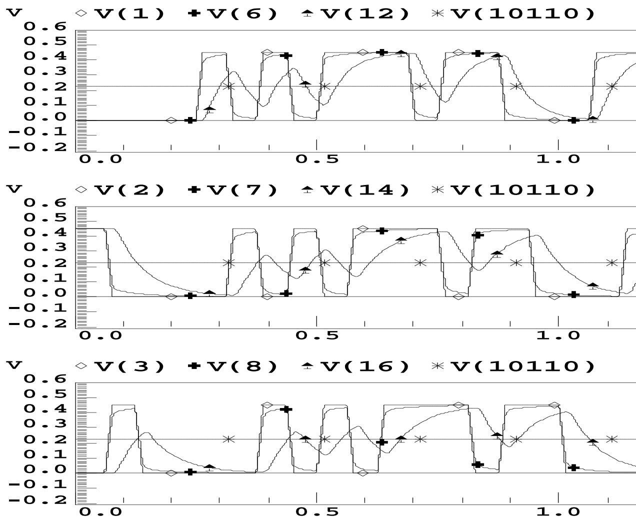

Figure 12: Near and Far End Signal in 35 nm Technology Without Inductive and Capacitive Coupling

that it is especially important to take into account the coupling effects also for test patterns.

5 Conclusions

We have shown the problem of testing using LFSR's in nanometer technologies applying smallest possible geometries prognosed by the SIA roadmap. The most important problems will be the very high delay of the lines as well as the crosstalk. In the nanometer age the resistance per unit length of a line system increases in such a way that the line delay will be so large that it is nearly impossible to transmit LFSR test patterns without an error through a line system longer than 0.5 mm. For lines shorter than 0.5 mm the pattern propagation can be expected to be fault free, whereas lines which are longer than 1 mm produce critical errors. In addition, crosstalk between lines will also play an important role and cannot be neglected. Thus, at-speed-testing with standard LFSR test patterns is impossible. The expected serious problems of testing 'monster' chips [9] in future designs with long lossy and coupled lines can be reduced by two ways only: we either have new test techniques (e.g. new cellular automatas, dividing into smaller testable blocks with short lines) or, if there is a need for testing chips at high frequencies, long line systems have to be implemented in larger geometries.

References

[1] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors*, 1999.

[2] F. Caignet, S. Delmas-Bendhia and E. Sicard, "The Challenge of Signal Integrity in Deep-Submicrometer CMOS Technology," *Proceedings of the IEEE*, vol. 89, no. 4, April 2001, pp. 556–573.

[3] H. Grabinski, "An Algorithm for Computing the Signal Propagation on lossy VLSI Interconnect Systems in the Time Domain," *VLSI Journal on Integration*, vol. 7, no. 1, April 1989, pp. 35–48.

[4] E. Grotelüschen, H. Grabinski, S. Rochel, T. Winkel, "LOSSYWIRE - A Model Implementation for Transient and AC Analysis of Lossy Coupled Transmission Lines in the Circuit Simulator ELDO," *International Journal of Electronics and Communications*, vol. 49, no. 1, 1995, pp. 37–43.

[5] E. Grotelüschen, L.S. Dutta, S. Zaage, "Full-wave Analysis and Analytical Formulas for the Line Parameters of Transmission Lines on Semiconductor Substrates," *VLSI Journal on Integration*, vol. 16, 1993, pp. 33–58.

[6] P. Nordholz, D. Treytnar, H. Grabinski, J. Otterstedt, D. Niggemeyer, U. Arz and T. W. Williams, "Signal Integrity Problems in Deep Submicron Arising from Interconnects between Cores," *Proceedings VLSI Test Symposium, VTS'98*, 1998, pp. 28–33.

[7] M. Rodgers, "Defect Screening Challenges in the Gigahertz/Nanometer Age," *Proceedings IEEE International Test Conference, ITC'2000*, 2000, pp. 464–467.

[8] P.H. Bardell, W.H. McAnney and J. Savir, "Built-In-Test for VLSI," *John Wiley & Sons*, 1987.

[9] Y. Zorian, "Testing the Monster Chip," *IEEE Spectrum*, vol. 36, no. 7, 1999, pp. 54–60.