Self-Configuration of a Large Area Integrated Multiprocessor System for Video Applications

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Abstract

We present a configuration technique for a Large Area Integrated Circuit (LAIC) which is manufactured by wafer stepping. A LAIC consists of four identical subsystems, i.e., a subsystem is the only building block of a LAIC and contains base cells or processing nodes as well as interconnects and pad cells. To ensure a proper cooperation of all subsystems and to enable communication between the subsystems, an on-chip self-configuration scheme is realized. Therefore, not only the subsystems are configured, but also the global bus system, connecting all subsystems.
Two methods for configuration are applied: static and dynamic. The processing nodes, the pad cells, and the input bus systems are configured statically. The output and the bidirectional bus system need a dynamic configuration, since they depend on the current state of the LAIC (e.g., which subsystem is accessing the bus).

The presented approach increases the area but enables to manufacture LAICs, consisting of only one building block, by wafer stepping with minimum configuration effort. The LAIC is manufactured in a standard 0.25 μm 6 metal layer embedded DRAM process with a die size of 16.89 cm^2.

1. Introduction

Several Wafer Scale Integration (WSI) systems and Large Area Integrated Circuits (LAICs) have been proposed to realize complex systems with high performance and high reliability. Wafer step/photocomposition techniques have been applied since the size of the design frame of a standard semiconductor manufacturing process is restricted. Thus, these systems had to be split into different parts or slices which can be repeated an appropriate number of times as building blocks in order to form a complete system [1], [2], [3]. These approaches utilized at least two different slices as building blocks, one for the base cell or processing node (PN) and one (or more) for the pads and the peripheral structures. However, these approaches caused difficulties in the manufacturing process that were not acceptable for large volume production, e.g., additional process steps [2], excessive number of laser links [2], or photocomposition [1], [2], [3]. In all previous approaches with photocomposition, the masks had to be partially blocked from exposure when repeating a certain slice, as the different slices have to be implemented on a single set of masks. The therefor required modification of the manufacturing process may not be allowed in a commercially available process.

The aim of our work was to implement a LAIC that is manufacturable in a standard semiconductor manufacturing processes without modification of the process and with minimum configuration

effort. Therefore, the LAIC has to be functional and fully configured without processing laser links or fuses in case it is defect free. Moreover, the LAIC has to be composed of a single building block.

The *AxPe*-LAIC is the implementation of a programmable video signal processing architecture with distributed embedded DRAM [4]. The architecture allows to employ an arbitrary number of video processing nodes to perform various video coding algorithms on video streams of different bandwidth according to the resolution of the video image. Each PN consists of a complex video processing core of the type *AxPe* [5], application specific interfaces, and 4MB embedded frame buffer memory. An *AxPe*-LAIC employing 16 PNs is manufactured in a commercially available 0.25 μm 6 metal layer embedded DRAM process. However, the complexity of the PN does not allow to implement more than 4 PNs within the design frame of this process. Thus, the building block of the *AxPe*-LAIC is a reticle-size subsystem which consists of 4 PNs, pad cells for every signal, pre-configured interconnects, self-configuration circuitry, and peripheral structures required for manufacturing to satisfy the restriction to a single building block. This building block is denoted *AxPe-Subsystem*. The die size of an *AxPe*-LAIC composed of 4 *AxPe-Subsystems*, i.e. 16 PNs, amounts to 16.89 cm^2. Figure 1 shows the floorplan of a PN, an *AxPe-Subsystem* consisting of 4 PNs, and an *AxPe*-LAIC consisting of 4 *AxPe-Subsystems*.

The remainder of the paper is organized as follows. In Section 2, the test strategy of the system is briefly reviewed and its defect tolerance scheme is presented. In Section 3, our new wafer step approach is introduced and design implications for the *AxPe Subsystem* are discussed. In Section 4, a technique is introduced that allows the individualization of the PNs and configuration of interconnect systems without individual lines for PNs and without programming of laser fuses. This

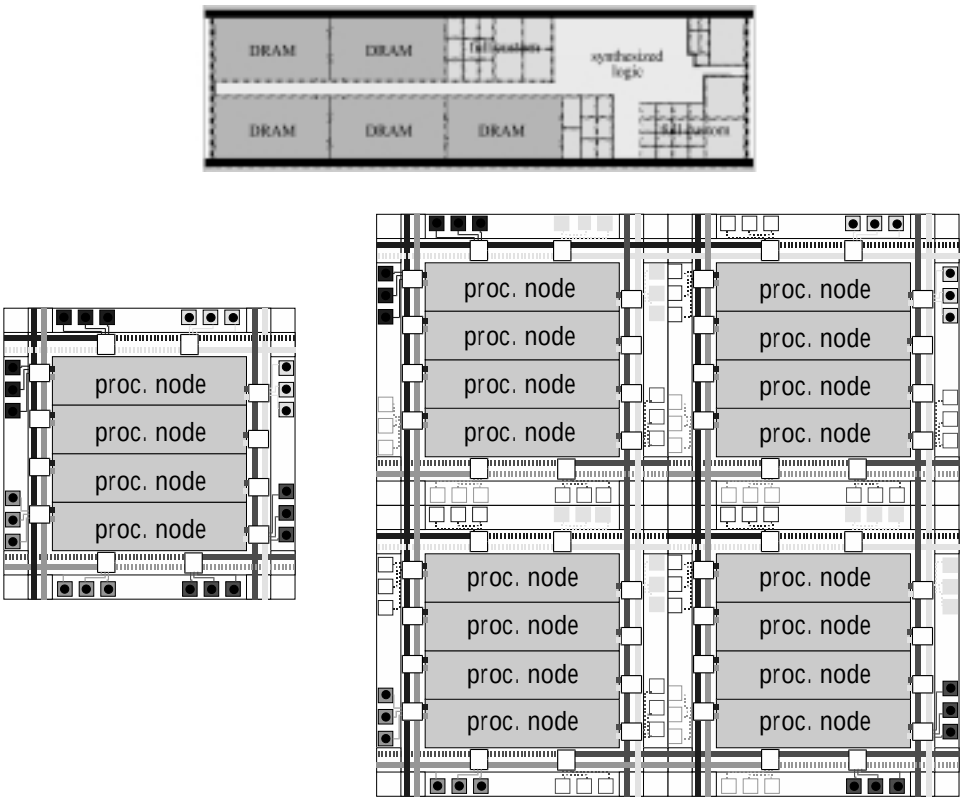

Figure 1. Floorplan of processing node (PN) (top), *AxPe-Subsystem* **(left bottom) and** *AxPe*-**LAIC (right bottom)**

technique can be extended to be applicable in interconnect systems where dynamic switching is required, e.g., in bi-directional bus systems, described in Section 5. Section 6 concludes the paper.

2. Test and yield enhancement issues

For the implementation of the *AxPe*-LAIC, both yield loss by manufacturing defects and soft errors occurring in the embedded DRAM have to be considered. Test and defect localization are prerequisites to employ redundancy for defect tolerance.

On top level of the system's hierarchy, 16 identical PNs are connected to common I/O bus systems which feature a redundant line for each line of the bus system. The redundant lines are routed in metal 6 above the correspondent lines of the bus system in metal 5. Thus, a 100 % redundancy is achieved without area overhead. Reconfiguration of the redundant bus systems is done by processing arrays of laser fuses and links similar to [6]. On top level, defective PNs can be switched off by deactivating system clocks and all input signals. Furthermore, defective PNs are disconnected from the interconnect system by setting all output buffers to a high-ohmic state to maintain the functionality of the remaining system. However, the total performance of the *AxPe*-LAIC is degraded in case of a defect in a PN.

Fault tolerance for each PN is realized in two ways. First, the embedded DRAM employs word line redundancy. The DRAM is configured after wafer test in the foundry similar to commodity DRAM. Furthermore, a (39, 32) SEC-DED Hamming code for the DRAM data was implemented to mask soft errors in the DRAM. Applying this error correction code (ECC) increases the physical memory size to 5 MB and the DRAM area by 37 %. Nevertheless, it was shown in [7] that the resulting yield loss is negligible due to the defect masking capabilities of the ECC.

Some of the submodules of the PNs feature a proven test strategy as they have been used in previous designs (*AxPe*-processing core [1]) or have been provided as intellectual property (IP) cores (DRAM controller, embedded DRAM). To minimize the test development time for this considerably complex system, the test strategy re-uses the pre-defined tests.

The test strategy can be summarized in chronological order: First, the top level bus systems are tested by means of a fault tolerant scan-path consisting of modified boundary scan cells which wrap each PN. After reconfiguration of the bus systems — if necessary —, a standard scan test is applied on the DRAM controller. Furthermore, this scan path allows the control of a pseudo-random Built-In Self-Test (BIST) of the embedded DRAM. Finally, a pseudo-random BIST is applied on the *AxPe* video processing core. All system registers of the processing core are replaced by self-testable BILBO registers [8] which can be employed as pseudo-random test pattern generators or as test signature generators. An integrated defect tolerant self-test controller determines the test phases of the AxPe processing core and evaluates the tests answers globally. If the BIST fails the PN is disconnected from the system by the BIST controller. All tests are executed for all PNs in parallel.

3. Implementation of the *AxPe*-LAIC

The *AxPe*-LAIC is manufactured by photocomposition of four *AxPe Subsystem*. To benefit from the scalability of the architecture, an arbitrary number can form a functioning *AxPe*-LAIC without changes in the manufacturing process or the set of masks. For instance, a single *AxPe-Subsystem* can be housed in a standard package and be employed for lower-resolution video coding. This feature has to be considered for the design of the *AxPe-Subsystem*. In this Section, we discuss the case of an *AxPe*-LAIC with 16 PNs as shown in Figure 1 (right bottom).

3.1. Pad cells

In contrast to previous LAICs where pad cells were realized on an extra slice, we have to integrate the pad cells on the *AxPe-Subsystem* to comply the single slice constraint. We implement pad cells for all signals which are placed equidistantly at all four edges since a single packaged *AxPe-Subsystem* has to be fully functional. We divide all bond pads in four groups corresponding to the four corners of the die: two groups for input signals (upper left and upper right corners), one group for output signals (lower left corner), and one group for bi-directional signals (lower right corner). Hence, the effort for the control logic of the bus repeaters is reduced. The different groups of signals are indicated by different shades of grey in Figure 1. Note, that on the *AxPe*-LAIC each element exists fourfold including the peripheral structures and all pad cells. The layout and placement of each of the four corresponding elements is identical. On the LAIC, only one of the four sets of signal pads is bonded, indicated by dots on the grey squares representing bonded signal pads in Figure 1 while on a packaged single *AxPe-Subsystem*, all signal pads are bonded. On an arbitrary LAIC, that set of pads is always bonded which is located at an outer corner of the die. One task of the configuration circuitry is to select one set of pad cells and deactivate the other three (see Section 4).

In contrast to signal pads, the number of power pads of an *AxPe-Subsystem* is dimensioned for the power requirements of a LAIC consisting of 4 *AxPe-Subsystems*. On a LAIC, only that half of the power pads can be bonded, which is localized at outer edges of the die. Therefore, twice as many power pads have to be implemented on an *AxPe-Subsystem* than being necessary for a packaged single *AxPe-Subsystem*. The design of the power distribution limits the maximum number of columns of subsystems to 2 on a LAIC. After fabrication, the power supply of adjacent subsystems is disconnected, while the substrate provides a common reference voltage level. Additionally, each PN is supplied independently. Thus, it is possible to disconnect each processing node from power supply in case that power shorts occur.

3.2. Floorplan

As indicated in Figure 1, the shape of a PN is chosen to be a rather narrow rectangle. This shape does not result in excessive internal signal delays of the processing nodes in our case but is advantageous for 1) the design of interconnects, 2) the design of power supply lines, and 3) the scaling of an *AxPe-Subsystem*. First, the result is a simple rectangular mesh topology for the interconnect systems. The interconnects are divided up in two horizontal and two vertical routing channels. Second, power lines are led horizontally on the *AxPe-Subsystems* and thus the power pads on the left (right) edge of the *AxPe-Subsystem* are connected to the left (right) edge of a PN (not shown in Figure 1). On a LAIC, the power pads at only one (the outer) edge of a *AxPe-Subsystem* can be bonded. Power rails that connect the power pins from the left to the right side of a PN limit the power supply loss from the outer edge to the inner edge to 0.2 V on a LAIC. The power rails are indicated by the horizontal black bars in Figure 1 (top). The peak power of a PN is estimated to be 1.1 W at 166 MHz. Third, the rectangular shape allows a straightforward extension from four PNs to five or more PNs per *AxPe-Subsystem* for future developments.

3.3. Interconnects

An *AxPe-Subsystem* has to contain a seal ring and process control blocks for compatibility to the manufacturing process. These peripheral structures and the ring of pad cells form a boundary that are crossed by interconnects in metal 6 which are routed to the edge of the design frame in horizontal and vertical direction. These interconnects are twice as wide as the minimum design rules to take

into account the stepping accuracy of the wafer stepper. By processing the masks of an *AxPe-Subsystem* with slight overlap in metal 6, a wafer is produced which is completely filled with fully connected *AxPe-Subsystems*. Appropriate sawing separates these *AxPe-Subsystems*. The system is scalable, as sawing out an arbitrary number of *AxPe-Subsystems* results always in a connected and functionable LAIC. The effects of double exposure is not a problem as has been proven in our earlier designs [1].

For the interconnect systems, a bus topology was required for the implemented architecture, not the mesh topology that is initially manufactured by photocomposition. Therefore, some interconnects have to be disabled in order to transform the mesh topology into a bus topology. The disabled interconnects are indicated by dashed lines in Figure 1. The resulting interconnect system shows lengths of up to 6 cm on the LAIC, e.g. from the top left pad cells to the lower right PNs. To maintain signal integrity on these long and parallel lines repeaters are mandatory for all signals. The repeaters are dimensioned and placed according to the results of extensive simulations of different bus topologies. Our simulation models were verified by HF measurements of full custom test structures manufactured in the same process [9]. The white rectangles in Figure 1 represent the arrays of laser fuses and links. These arrays also provide a pre-configured connection of the pad cells to the interconnect system.

3.4. Area overhead

The drawback of our approach is the extra cost in terms of silicon area due to unused elements, as PCBs and pad cells at the inner edges of an *AxPe*-LAIC, and of the disabled parts of the interconnects. An additional area overhead of about 12.5 % is expected, compared to a *AxPe-Subsystem* with 16 PNs. However, we gain the simplification of the wafer step process and the flexibility to obtain LAICs with an arbitrary number of PNs.

4. Static configuration techniques

The composition of the *AxPe*-LAIC out of a single building block results in multiple sets of bond pads. Only one of these sets has to be bonded while the others must not affect the functionality of the system and have to consume minimum power. Furthermore, the manufactured mesh of interconnects has to be configured to establish a bus topology. Finally, PNs with identical layout are accessed in parallel. Nevertheless, they have to be distinguishable for programming as every PN performs different tasks. Therefore, a simple self-configuration circuitry is used, which restricts the processing of laser fuses and links to repairing defects.

4.1. Pad cells

Figure 1 indicates that three of four pad cells of the *AxPe*-LAIC are not bonded. These pads are not necessary for the system and have to be disconnected from the interconnect systems. A static configuration pad cell with pull-down resistor is added at each edge of the *AxPe-Subsystem* (see Figure 2). This pad is always bonded if it lies at an outer edge of the LAIC die. Thus, inner and outer edges can be distinguished since the unbonded configuration pads at the inner edges keep the low voltage level while the bonded configuration pads at the outer edges are externally driven to the high voltage level. The output of two configuration pad cells at two adjacent edges are ANDed to enable the correspondent signal pad cells. Therefore, pad cells which belong to a set at the corners of a LAIC-die are connected to the bus system while all others are disabled. It is impractical to separate unused pad cells from power supply to reduce power consumption as we

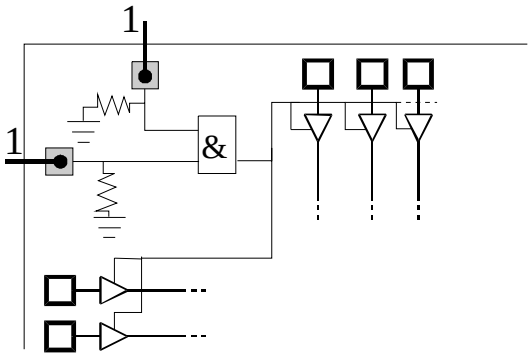

Figure 2. Automatic selection of pad cells

utilize standard-cells from a commercial library. However, the pull down resistors prevent these cells from switching and dynamic power consumption. In case of a defect in this configuration circuitry, the control signal can be set by processing a single pair of a laser link and a laser fuse.

Note, that on a single packaged *AxPe-Subsystem*, all edges are outer edges. Thus, all configuration pad cells are bonded and all signal pads are enabled.

4.2. Bus systems

Similar to unused pad cells, open ends of interconnects at outer edges have to be disabled statically as they may float at an unknown voltage level. Therefore, the bus repeaters — originally intended for signal integrity — are implemented as tri-state buffers. To control these buffers, the output signals of the configuration pad cells at the top edge and at the left edge are utilized.

These two signals supply a non-ambiguous information about the position of each subsystem on the LAIC (’11’ for the upper left subsystem, ’10’ for the upper right, ’01’ for the lower left, and ’00’ for the lower right). As the configuration of the interconnect system depends on this position only, these static configuration signals are sufficient to enable or disable parts of the interconnect system according to Figure 1 by adding a few logic gates. Again, laser fuses and links are provided for fault tolerance.

4.3. Numbering of processing nodes

In video signal processing, all PNs perform different tasks. In particular, they process different segments of the video image independently. The identical PNs are individualized to allow for individually addressing the nodes by using the static configuration pads. Their output signals are stored in a configuration register in each PN. Two additional configuration bits differentiate the PNs on each subsystem. As these two bits can be identical on different subsystems, they are hard wired.

The combination of the configuration bit pair with the locally generated bit pair provides a non-ambiguous numbering of the PNs on a *AxPe*-LAIC. For programming of the *AxPe*-LAIC, each code or word can be sent together with a 4bit receiver code in parallel to all PNs. By comparing the receiver code to the stored PN number, each PN can be accessed independently.

But the described method of numbering becomes ambiguous for more than two rows or columns of subsystems. The extension of the configuration circuitry given in Figure 3 solves this problem. In this case, configuration signals have to be transferred between adjacent subsystems similar to input or output signals. A circuitry with two configuration pins allows to distinguish, three rows of *AxPe-Subsystems*. This scheme is scalable for any desired number of rows by simply adding an

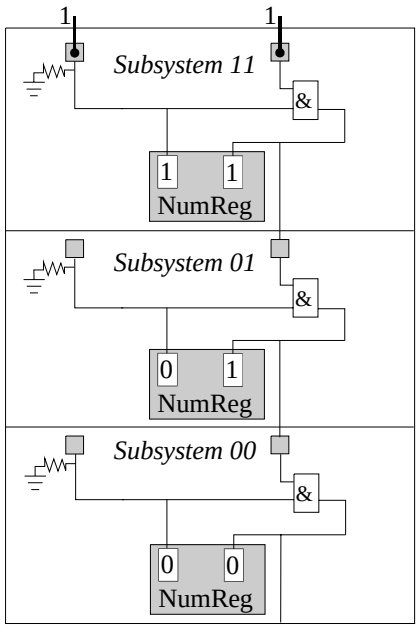

Figure 3. Circuitry for numbering of *AxPe-Subsystems*

appropriate number of configuration pins and can be applied for the horizontal direction in the same way resulting in a non-ambiguous numbering of PNs in arbitrary LAICs.

5. Dynamic configuration techniques

To make simple self-configuration techniques applicable on the LAIC, complex switched interconnect networks had to be avoided. Thus, the global bus systems are partitioned in plain input and output bus systems with one exception: a 16 bit bi-directional inter-PN communication bus which was required from system architecture. As shown in Section 3, bus repeaters are required to ensure signal integrity. The repeaters have to be controlled to establish certain signal paths across the LAIC by changing their direction.

Input and output bus systems can be considered as a subset of bi-directional bus systems, so we will focus on the latter. From system topology, a bi-directional interconnect system has to provide five different signal paths on a *AxPe*-LAIC given in Figure 4: an external host IC transmits and all PNs receive (Figure 4 a), or a PN on one of the *AxPe-Subsystems* transmits and all other receive as well as the external host IC (Figures 4 b to e). Note that for all cases the same parts of the interconnect system are used forming an upside-down turned 'U' (static configuration) while all repeaters may change their direction dependent on the state of the system, i.e., which subsystem is accessing the bus. The signal flow is not affected by defective PNs as they are separated from the bus system by local tri-state buffers, not shown in Figure 4 (see Section 2). The five different cases of signal flows on the *AxPe*-LAIC can be mapped on the inout bus system with bi-directional repeaters given schematically in Figure 5. The repeaters are placed next to the crossing of horizontal and vertical interconnects except for the drivers of the bond pad signals as indicated in Figure 5. Thus, all requirements concerning the maximum line length driven by a repeater and the necessary signal flow directions can be fulfilled by the presented set of four bi-directional repeaters per I/O-signal and per *AxPe-Subsystem*. Repeaters with white background are permanently deactivated by the

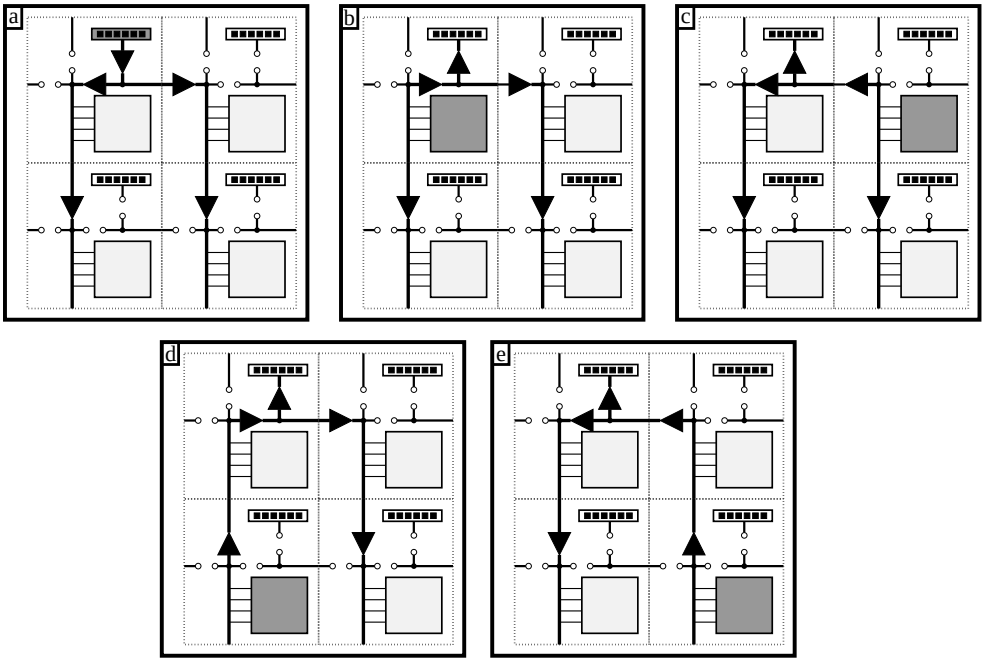

Figure 4. Signal flow of bi-directional bus system with host-IC as source (a) and different subsystems as source ((b) to (e))

static individualization (see Section 4). Repeaters with light grey background are active and may change direction depending on the current signal flow. To control the direction of the repeaters, the current state of the system (e.g., which subsystem is writing to the bus) is superimposed to the static configuration by few logic gates. The current state is determined and held locally on each PN. Therefore, each subsystem has to report its current state to the repeater control circuitry of its left and of its upper neighbor. The timing of the control circuitry is not critical as all bus systems run asynchronically at a reduced external clock rate. The implemented approach is applicable to arbitrary LAICs as the control of the bus repeaters only differs for the first row of subsystems and all other rows or for the first column and all other columns respectively.

6. Conclusions

In this work, we presented a 16.89 cm^2 Large Area Integrated Circuit (LAIC) which is realized by a novel approach of wafer stepping. In this approach, the LAIC is composed of a single building block that is designed as a complete chip with all pad cells and other periphery. In spite of significant area overhead, this technique is advantageous since the manufacturing process becomes feasible. In particular, neither processing of laser fuses or links nor blocking of parts of the masks from exposure is required. Instead, we developed a special topology for the global bus systems and processing nodes and a simple self-configuration circuitry. This circuitry considers dynamically switched I/O bus systems and defective processing nodes. Although our wafer stepping and self-configuration approach was developed for the *AxPe*-LAIC, it is generally applicable to similar WSI systems.

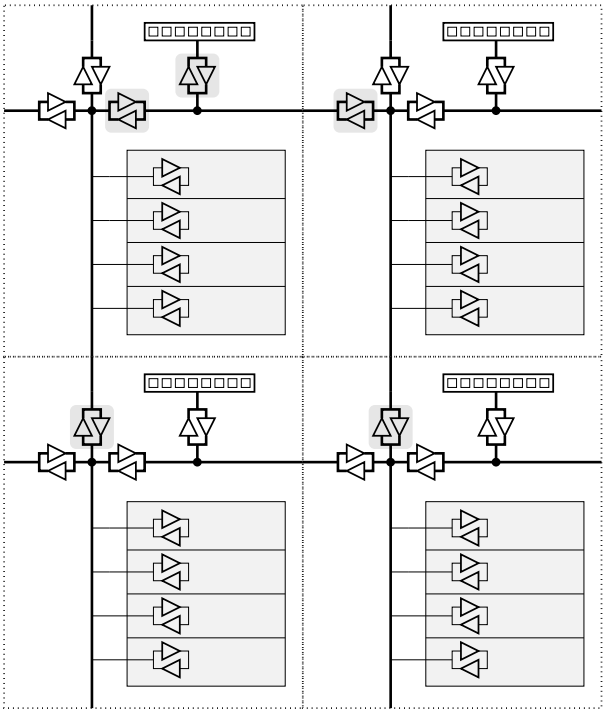

Figure 5. Schematic representation of inout bus with bi-directional repeaters

Acknowledgments

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